PROGRESS & NEXT

From Our Own NPU to Our First AI Chip.

Turning design assets into silicon and systems.

2026.01 — **Proprietary NPU Core developed**
SUAI · Samsung Foundry 28 nm

2026.06 — **SUAI NPU silicon received**
NPU chip packaging

2026.08 — **First AI chip design**
Sem-V1 · Samsung Foundry 28 nm

NOW — **Board build & validation underway**
Voice functions · Power · PPA evaluation

Dec-Feb 2026-27 — **VUI v2 · SLM tape-out**
Expected schedule

2027.03 Expected — **Receipt of first AI chip (Sem-V1)**
Expected · Integrated validation upon receipt

NEXT / DEVELOPMENT DIRECTION

VUI Evolution
Revised NPU + SoC optimization

SLM
Transformer compute optimization

Vision
Planned

PRODUCT & BUSINESS

NPU IP and AI Chips. Two Supply Paths.

Pursuing IP licensing and chip supply in parallel, built on shared NPU assets

01 IP Licensing

For MCU · SoC chipmakers

An integrated offering of target AI models, NPU IP and CPU interface SW

Licensing · Integration Support

02 AI Chip Sales

Our first AI chip, built on our own NPU

Wake-up chips running target AI models
Supply planned after evaluation and validation

Chip Sales · Paid PoC

(03) AI Solution Service

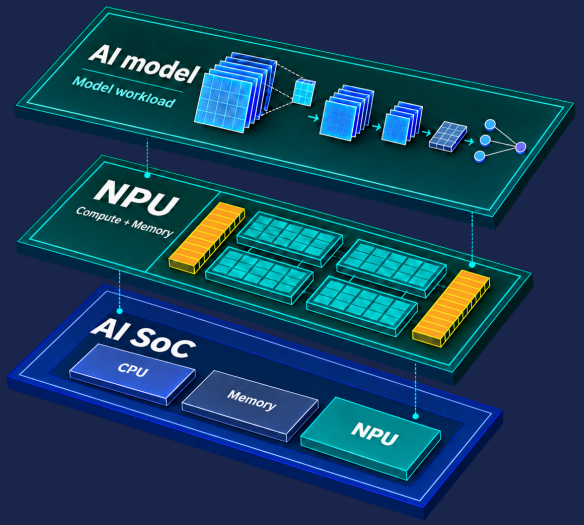
Co-developing models, runtime SW and device integration
Projects focused on core products and future IP

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PURPOSE-BUILT NPU & AI SoC

AI Chips Optimized for Your AI Models

- Ultra-compact NPU
- Super-low Power
- Purpose-built



FIRST APPLICATION

ASR/VOICE AI

(Automatic Speech Recognition)

First Application: ASR/VOICE AI

We are developing an on-device voice interface (VUI) to detect wake words and selected predefined phrases.

FIRST SCOPE / INITIAL DEVELOPMENT



Implementation scope will be validated by product.
NLU: extension under evaluation

AI MODEL FIT

Model Requirements	Product Requirements
Accuracy · Compute Memory	Avg. Power · Size Component Cost

TARGET CUSTOMERS

MCU · SoC Chipmakers

Companies seeking to integrate voice AI into their chips

Potential applications for our chips:
Appliances · Smart Plugs · Wearables

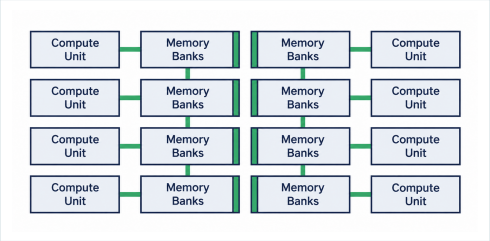
NOW / Customer outreach · Evaluation preparation

Model · NPU · SW Designed Together

PIM-like NPU

We combine close placement of memory and compute with a reconfigurable NPU architecture.

Zero-skipping NPU Core revision in progress



Concept: close placement of compute and memory

01 **Purpose-built**

Designed for target AI model workloads and product requirements

02 **Power-efficient**

Optimizing compute, memory and execution paths to reduce power consumption

03 **Ultra-compact**

Using proprietary IP and Physical Design to optimize cost and size

NPU (Simulation)

0.15 ~ 2 TOPS **6-8 TOPS/W**

INT8 · Scalable

Simulation reference; not measured product specifications.

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LET'S BUILD WHAT'S NEXT

Next: Validate Products and Win First Customers.

Building on our NPU silicon experience, we are pursuing voice AI product validation and commercialization.

01 **Hardware Validation**

Recognition quality · Inference energy
Average system power

02 **Customer Acquisition**

IP Sales · Paid PoC

03 **Productization**

Preparing functional compact chip modules and a customer integration support package

TECHNICAL PARTNERSHIPS · INVESTMENT

contact@semunite.com

www.semunite.com

Semunite Inc.